CLAIMS

What is claimed is:

1. An apparatus, comprising:

control logic comprising a plurality of logic cells, at least one of the plurality of logic cells configured to receive an A operand and a B operand and perform the following logic operations comprising $\overline{A}B$, $A\overline{B}$, and AB; and

switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the result of the AB logic operation.

2. The apparatus of claim 1, wherein the control logic is coupled to receive a first plurality of enable signals, each of the first plurality of first enable signals corresponding to a first plurality of one or more bits of a first segment of the input data, and wherein the control logic is coupled to receive a second plurality of enable signals, each of the second plurality of enable signals corresponding to a second plurality of one or more bits of a second segment of the input data.

3. The apparatus of claim 2, wherein the plurality of logic cells are coupled in a matrix of N columns and M rows comprising:

a first row of logic cells, each of the logic cells in the first row having first inputs to receive a corresponding one of the first plurality of enable signals, wherein a first one of the logic cells in the first row has an input coupled to receive a first one of the second

plurality of enable signals, wherein N-1 number of succeeding logic cells in the first row have second inputs coupled to receive the result of the $\overline{AB}$ logic operation of a preceding logic cell in the first row as the B operand; and

a first column of logic cells, each of the logic cells in the first column having first inputs to receive a corresponding one of the second plurality of enable signals, wherein a first one of the logic cells in the first column has an input coupled to receive a first one of the first plurality of enable signals, wherein M-1 number of succeeding logic cells in the first column have second inputs coupled to receive the result of the $A\overline{B}$ logic operation of a preceding logic cell in the first column as the A operand, wherein each of the logic cells in the first column provides the result of the AB logic operation.

4. The apparatus of claim 3, wherein the switch circuitry further comprises:

a first plurality of multiplexers, each of the first plurality of multiplexers coupled to receive the result of the AB logic operation of the first and second columns of logic cells as control inputs, wherein each of the first plurality of multiplexers is coupled to receive the second plurality of one or more bits of the second segment of the input data, each of the first plurality of multiplexers to selectively output one of the second plurality of one or more bits of the second segment based on the result of the AB logic operation of the first and second columns of logic cells.

5. The apparatus of claim 4, wherein the switch circuitry further comprises:

a second plurality of multiplexers, each of the second plurality of multiplexers coupled to receive a corresponding one of the first enable signals as a control input,

wherein each of the plurality of second multiplexers is coupled to receive a corresponding one of the first plurality of one or more bits of the first segment as a first input and the selected output of a corresponding one of the first plurality of multiplexers as a second input, each of the second plurality of multiplexers to selectively output one of the first and second inputs based on the control input.

6. The apparatus of claim 2, wherein the at least one of the plurality of logic cells has a first input, a second input, a first output, a second output and a third output, and

wherein the first input is coupled to receive a first one of the plurality of first enable signals as the A operand, wherein the second input is coupled to receive a first one of the plurality of second enable signals as the B operand, wherein the first output provides the result of the $\overline{A}B$ logic operation, wherein the second output provides the result of the $A\overline{B}$ logic operation, and wherein the third output provides the result of the AB logic operation.

7. The apparatus of claim 6, wherein the plurality of logic cells comprises:

a first logic cell comprising the at least one of the plurality of logic cells;

a second logic cell, the second input of the second logic cell coupled to receive the result of the $\overline{A}B$ logic operation from the first logic cell as the B operand of the second logic cell, the first input of the second logic cell coupled to receive a second one of the plurality of first enable signals as the A operand of the second logic cell, the third output of the second logic cell to provide the result of the AB logic operation of the second logic cell;

a third logic cell, the second input of the third logic cell coupled to receive a second one of the plurality of second enable signals as the B operand of the third logic cell, the first input of the third logic cell coupled to receive the result of the $A\overline{B}$ logic operation of the first logic cell as the A operand of the third logic cell, the third output of the third logic cell to provide the result of the AB logic operation of the third logic cell; and

a fourth logic cell, the second input of the fourth logic cell coupled to receive the result of the $\overline{A}B$ logic operation from the third logic cell as the B operand of the fourth logic cell, the first input of the fourth logic cell coupled to receive the result of the $A\overline{B}$ logic operation of the second logic cell as the A operand of the fourth logic cell, the third output of the fourth logic to provide the result of the AB logic operation of the fourth logic cell.

8. The apparatus of claim 7, wherein the switch circuitry comprises:

a first multiplexer having control inputs coupled to receive the result of the AB logic operation from the first and third logic cells, the first multiplexer having inputs coupled to receive the first plurality of one or more bits of the second segment of the input data, the first multiplexer to selectively output one of the first plurality of one or more bits of the second segment of the input data based on the result of the AB logic operation from the first and second logic cells; and

a second multiplexer having control inputs coupled to receive the result of the AB logic operation from the fourth and second logic cells, the second multiplexer having inputs coupled to receive the first plurality of one or more bits of the second segment of

the input data, the second multiplexer to selectively output one of the first plurality of one or more bits of the second segment of the input data based on the result of the AB logic operation from the first and second logic cells.

9. The apparatus of claim 8, wherein the switch circuitry further comprises:

a third multiplexer having a control input coupled to receive the first one of the plurality of first enable signals, the third multiplexer having a first input coupled to receive one of the first plurality of one or more bits of the first segment of input data, the third multiplexer having a second input coupled to receive the output of the first multiplexer, the third multiplexer to selectively output either the one of the first plurality of one or more bits of the first segment of input data or the output of the first multiplexer based on the first one of the plurality of first enable signals; and

a fourth multiplexer having a control input coupled to receive the second one of the plurality of first enable signals, the fourth multiplexer having a first input coupled to receive another of the first plurality of one or more bits of the first segment of input data, the fourth multiplexer having a second input coupled to receive the output of the second multiplexer, the fourth multiplexer to selectively output either the another of the first plurality of one or more bits of the first segment of input data or the output of the second multiplexer based on the second one of the plurality of first enable signals.

10. The apparatus of claim 3, wherein the control logic comprises matrix of N columns and M rows of logic cells, where N is equal to a number of the first plurality of enable signals and M is equal to a number of the second plurality of enable signals.

11. The apparatus of claim 1, further comprising:

a content addressable memory (CAM) array coupled to receive the comparand; and

a filter circuit coupled to the CAM array, the filter circuit comprising the switch circuitry and the control logic, wherein the filter circuit is coupled to receive the input data and transpose the one or bits of the input data from an initial position in the input data to a different position in the comparand relative to other bits of the input data that are transposed to the comparand.

12. The apparatus of claim 11, wherein the input data has a first data segment and a second data segment and wherein the filter circuit is configured to replace one or more bits of the first data segment with one or more bits from the second data segment to form the comparand.

13. The apparatus of claim 12, further comprising a comparand register coupled between the CAM array and the filter circuit to store the comparand.

14. The apparatus of claim 1, wherein at least another of the plurality of logic cells is configured to receive a result of the $\overline{AB}$ logic operation of the at least one logic cell and an enable signal as the B operand, and wherein the at least another of the plurality of logic cells is configured to perform the AB logic operation.

15. A method, comprising:

providing a matrix of M rows and N columns of logic cells in a content addressable memory (CAM) device, where N is equal to or greater than 1 and M is greater than 1; and

performing an AB logic operation in each of the logic cells.

16. The method of claim 15, further comprising:

selecting among a second one or more bits of input data using a result of the AB logic operation in at least one of the logic cells; and

selecting between the selected second one or more bits of input data and a first one or more bits of input data for output to a comparand in the CAM device.

17. The method of claim 16, further comprising:

receiving a first enable signal as an A operand in a first one of the logic cells, the first enable signal corresponding to the first one or more bits of input data; and

receiving a second enable signal as a B operand in the first one of the logic cells, the second enable signal corresponding to the second one or more bits of input data.

18. The method of claim 17, further comprising:

performing an $\overline{A}B$ logic operation in the first logic cell and providing a result of the $\overline{A}B$ logic operation as a B operand to a second logic cell; and

performing an $A\overline{B}$ logic operation in the first logic cell and providing a result of the $A\overline{B}$ logic operation as an A operand to a third logic cell.

19. The method of claim 18, wherein performing the AB logic operation in at least one of the logic cells comprises:

performing the AB logic operation in the first logic cell to generate a first result; and

performing the AB logic operation in the second logic cell to generate a second result.

20. The method of claim 19, wherein selecting among the second one or more bits of input data using the result of the AB logic operation comprises using at least one of the first and second results to select among the second one or more bits of input data.

21. The method of claim 20, wherein selecting between the selected second one or more bits of input data and the first one or more bits of input data for output to the comparand comprises using the received first enable signal.

22. The method of claim 17, wherein performing the AB logic operation in each of the logic cells comprises:

performing the AB logic operation in each of a N number of logic cells in the first row of the matrix of logic cells using the A operand; and

performing the AB logic operation in each of a M number of logic cells in a first column of the matrix of logic cells using the B operand.

23. The method of claim 22, wherein performing the AB logic operation in each of the logic cells further comprises:

performing the following logic operations in each of an M-1 number of logic cells in each of the M rows and each of an N-1 number of logic cells in each of the N columns: an $\overline{A}B$ logic operation and an $A\overline{B}$ logic operation;

receiving a result of the $\overline{A}B$ logic operation of a preceding logic cell in a row of the M rows as the B operand in a succeeding cell in the row and performing the AB logic operation in the N-1 number of succeeding logic cells in the row; and

receiving a result of the $A\overline{B}$ logic operation of a preceding logic cell in a column of the N columns as the A operand in a succeeding cell in the column and performing the AB logic operations in the M-1 number of succeeding logic cells in the column.

24. A content addressable memory (CAM) device, comprising:

a matrix of M rows and N columns of logic cells, where N is equal to or greater than 1 and M is greater than 1; and

means for performing an AB logic operation in each of the logic cells.

25. The CAM device of claim 24, further comprising:

means for selecting among a second one or more bits of input data using a result of the AB logic operation in at least one of the logic cells; and

means for selecting between the selected second one or more bits of input data and a first one or more bits of input data for output to a comparand in the CAM device.

26. A content addressable memory (CAM) device, comprising:

a CAM array coupled to receive a comparand; and

a filter circuit coupled to the CAM array, wherein the filter circuit is coupled to receive input data, the input data including a first one or more bits having a first order position and a second one or more bits having a second order position being one of lower than or higher than the first order position, wherein the filter circuit is configured to provide the first one or more bits to the comparand in the first order position and transpose the second one or bits of the input data to a third order position in the comparand, the third order position being the other of the lower than or higher than the first order position.

27. The CAM device of claim 26, wherein the second order position is higher than the first order position, and wherein third order position is lower than the first order position.

28. The CAM device of claim 26, wherein the second order position is lower than the first order position, and wherein third order position is higher than the first order position.

29. The CAM device of claim 26, wherein the filter circuit is configured to replace a third one or more bits of the input data having the third order position in the input data with the second one or more bits into the third order position in the comparand.

30. The CAM device of claim 26, further comprising a comparand register coupled between the CAM array and the filter circuit to store the comparand.

31. The CAM device of claim 26, wherein the filter circuit comprises:

switch circuitry coupled to receive the input data; and

control logic coupled to the switch circuitry.

32. The CAM device of claim 31, wherein the control logic comprises a plurality of logic cells, each configured to receive an A operand and a B operand and perform an *AB* logic operation.

33. A method in a content addressable memory (CAM) device, comprising:

receiving input data including a first one or more bits having a first order position and a second one or more bits having a second order position being one of lower than or higher than the first order position;

providing the first one or more bits to a comparand in the first order position; and

transposing the second one or bits of the input data to a third order position in the comparand, the third order position being the other of the lower than or higher than the first order position.

34. The method of claim 33, wherein the second order position is higher than the first order position, and wherein third order position is lower than the first order position.

35. The method of claim 33, wherein the second order position is lower than the first order position, and wherein third order position is higher than the first order position.